WHAT IS CLAIMED IS:

1. A layout design apparatus for carrying out layout design of a semiconductor integrated circuit, said layout design apparatus comprising:

a region decision section for determining, in the semiconductor integrated circuit including a first circuit and a second circuit, a first circuit region to be assigned to the first circuit and a second circuit region to be assigned to the second circuit;

an initial layout section for carrying out placement and routing using a netlist of the entire semiconductor integrated circuit such that a layout of the first circuit whose wiring consists of n wiring layers is formed in the first circuit region, where n is an integer equal to or greater than two, and that a layout of the second circuit, which has wiring consisting of (n-m) wiring layers and is connected to the layout of the first circuit, is formed in the second circuit region, where m is a positive integer less than n; and

a layout modifying section for carrying out placement and routing using a netlist of a third circuit to form a layout of the third circuit such that wiring of the third circuit consists of the (n-m) wiring layers constituting the wiring of the second circuit, and for replacing the layout of the second circuit formed by said initial layout section by the layout of the third circuit.

2. The layout design apparatus according to claim 1, wherein said layout modifying section comprises:

a netlist creating section for creating the netlist of the third circuit;

a placement and routing section for carrying out the

placement and routing using the netlist of the third circuit to form the layout of the third circuit such that the wiring of the third circuit consists of the (n-m) wiring layers constituting the wiring of the second circuit; and

a connecting section for replacing the layout of the second circuit formed by said initial layout section by the layout of the third circuit, and for connecting the layout of the third circuit to the layout of the first circuit.

3. The layout design apparatus according to claim 1, wherein the layout of the third circuit is connectable to the layout of the first circuit using the wiring connecting the layout of the second circuit to the layout of the first circuit.